REMARKS

I. Introduction

In the Office Action of August 5, 2003, the independent claims were again rejected under 35 U.S.C. § 103(a) in view of the proposed combination of (1) U.S. Patent No. 6,208,545 to Leedy and European Patent Application No. EP1017100 to Shimoda et al., (2) Leedy and U.S. Patent No. 5,835,396 to Zhang, and (3) Leedy and U.S. Patent No. 6,034,882 to Johnson et al. Each of the independent claims contained the term "chip," and, in the Office Action, the Examiner stated that the previous acceptance of Applicants' definition of "chip" was withdrawn. The Examiner suggested that Applicants specifically recite what it considers to be a difference between the claimed invention and the cited art instead of relying on the definition of the term "chip." In this Amendment, Applicants have taken the Examiner's suggestion and have cancelled the rejected claims in favor of new claims that recite specific features instead of using the term "chip." The following sections discuss these amendments and why the pending claims are patentable over the cited art.

II. New Claims 125-140

In this Amendment, Applicants have cancelled the rejected claims and have replaced them with new Claims 125-140. Similar to the cancelled claims, the new claims relate to ECC and three-dimensional memory arrays. However, instead of using the term "chip," each of the independent claims (Claims 125, 129, and 134) recites the elements that the Examiner suggested be placed in the claims. Specifically, each of the independent claims recites a memory array comprising a plurality of memory cells arranged in a plurality of layers stacked vertically above one another, ***wherein the memory cell layers are deposited, patterned, and etched without using any bonding material between the memory cell layers***.

Support for this amendment is found, *inter alia*, in Figures 6A-6G; col. 4, lines 36-51; col. 11, line 42 – col. 16, line 49; and the abstract of U.S. Patent No. 6,034,882, as well as Figures 1-5; page 4, line 2 – page 5, line 8; page 6, line 9 – page 23, line 2; and the abstract of U.S. patent application serial number 09/560,626. Both of those patent documents were incorporated by reference on page 3 of the present application. To make clear that that disclosure is part of the present application, Applicants have amended the specification to include the above-cited drawings and description. Applicants have changed the figure numbers and some of the reference numbers for consistency. Because these documents were previously incorporated by reference, no new matter is being presented with this Amendment.

The added description and figures show two sets of embodiments: a pillar three-dimensional memory and a rail-stack three-dimensional memory. In each of these embodiments, one layer of memory cells is added over another layer of memory cells without gluing the layers together. For example, Figures 12(b)-(g) and the accompanying description show how subsequent layers of memory cells are deposited, patterned, and etched without using any bonding material between the memory cell layers.

III. The Claims Are Patentable Over the Art of Record

Three proposed combinations were used to reject the previously-pending independent claims: (1) Leedy and Shimoda et al., (2) Leedy and Zhang, and (3) Leedy and Johnson et al. Applicants submit that the new claims are patentable over each of these proposed combinations.

A. Leedy and Shimonda et al.

Each of the independent claims recites a memory array comprising a plurality of memory cells arranged in a plurality of layers stacked vertically above one another, ***wherein the memory***

cell layers are deposited, patterned, and etched without using any bonding material between the memory cell layers. Neither Leedy nor Shimoda et al. teaches this element.

With respect to Leedy, it was admitted on page 3 of the Office Action that "the three dimensional circuit [in Leedy] is constructed by ***bonding multiple substrate layers using thermal diffusion metal bonding***" (emphasis added).[1] Accordingly, Leedy does not deposit, pattern, and etch memory cell layers ***without bonding***, as recited in the claims.

In attempt to cure this deficiency, it was proposed to combine Leedy with Shimoda et al. However, like Leedy, Shimoda et al. fails to teach depositing, patterning, and etching memory cell layers without using any bonding material between the layers. See, for example, Figure 14 of Shimoda et al., which shows a conductive adhesive layer 22 between two separately-formed memory cell layers. Further, several passages in Shimoda et al. explicitly state that the disclosed memory cell layers are bonded together after manufacturing:

> Col. 22, lines 26-30: "the transfer source layer 42 formed on the substrate 1 and the transfer source layer 41 transferred to the substrate 21 ***are bonded (joined) to each other with a conductive adhesive layer 22 therebetween***" (emphasis added).
>
> Col. 31, lines 21-26: "the substrate 21 and the memory cell array 71, the memory cell array 71 and the memory cell array 72, and the memory cell array 72 and the memory cell array 73 may be ***bonded (joined)*** in any one of the methods according to the first to third examples" (emphasis added).

Other passages make clear that the memory cell layers in Shimoda et al. are fabricated individually and transferred to and bonded with other memory cell layers:

> Col. 23, lines 36-37: "each of the thin film device layers can be fabricated individually"

[1] See col. 3, line 66 – col. 4, line 12, in which Leedy defines his three-dimensional structure as a stack of integrated circuit layers that are ***bonded together***.

Front page abstract: ". . . a method for transferring a thin film . . . irradiating the separable layer . . . so that the thin film device layer on the support substrate is transferred to the substrate 21."

Col 1, lines 51-56: "A three-dimensional device . . . in which at least one of the thin film device layers is deposited by a transfer method."

Col 2, lines 4-5: ". . . at least one of the thin film device layers is deposited by a transfer method."

Col 2, lines 6-14: "A three-dimensional device . . . in which the transfer method includes . . . a thin film device layer on a support substrate . . . so that the thin film device layer . . . is transferred to a substrate of the three-dimensional device."

Col 6: The "best mode" text describes, once again, the transfer method. Lines 40-46 describe the necessity for transparency to light, as the best mode employs (laser) light to affect the separation of the thin films from the separate transfer source substrates. Once so liberated, the thin films are assembled atop the main recipient substrate to form the 3D device.

Col. 23, lines 1-4: "The substrate 1 is then separated from the substrate 21. Thus, as shown in Fig. 15, the transfer source layer 42 is detached from the substrate 1 and is transferred to the transfer source layer 41."

In summary, in both Leedy and Shimoda et al., the disclosed "three dimensional" structure is nothing more than a stack of individual memory cell layers that are assembled and bonded together at some point after manufacturing. Accordingly, the proposed combination of Leedy and Shimoda et al. fails to teach memory cell layers that are deposited, patterned, and etched without using any bonding material between the memory cell layers, as recited in the claims.

B. Leedy and Zhang or Johnson et al.

Each of the independent claims was also rejected in view of the proposed combination of Leedy and Zhang or Leedy and Johnson et al. Applicants respectfully submit that one skilled in

the art would not have been motivated to combine Leedy with Zhang or Johnson et al. to yield the claimed invention.

Put in the proper perspective, the claimed invention can be seen as a non-obvious evolutionary advance over Leedy, Johnson et al., and Zhang. Leedy shows bonded-together memory arrays with ECC but does not disclose a memory array with memory cell layers that are deposited, patterned, and etched without using any bonding material between the memory cell layers. Johnson et al. and Zhang disclose such a memory array but do not show the use of ECC. The claimed invention takes the step not contemplated by Leedy, Johnson et al., or Zhang — combining ECC with a memory array having memory cell layers that are deposited, patterned, and etched without using any bonding material between the memory cell layers.

Further, there is no suggestion to combine the references to yield the claimed invention. In the Office Action, it was asserted that one skilled in the art would have been motivated to replace the stacked integrated circuit memory disclosed in Leedy with the memory array taught in Johnson et al. or Zhang because of the advantages discussed in those patents. Applicants respectfully disagree because such a modification would change the basic operating principle of Leedy. Clearly, the primary focus of Leedy is his stacked integrated circuit memory, with ECC being merely an ancillary feature. Given the importance Leedy places on his particular memory, replacing the disclosed stacked integrated circuit memory with the memory in Johnson et al. or Zhang would change the basic operating principle of Leedy. As such, Applicants respectfully submit that one skilled in the art would not have been motivated to combine Leedy with Johnson et al. or Zhang to yield the claimed invention.

IV. Double Patenting Rejections

The claims were also rejected under the judicially-created doctrine of obviousness-type double patenting in view of the claims in U.S. Patent No. 6,545,891 to Tringali et al. In response to these rejections, Applicants submit herewith the appropriate terminal disclaimer and fee. In view of these submissions, Applicants respectfully request that the obviousness-type double patenting rejections be removed.

V. Conclusion

In view of the foregoing amendments and remarks, Applicants submit that this application is in condition for allowance. Reconsideration is respectfully requested. If there are any questions concerning this Amendment, the Examiner is asked to phone the undersigned attorney at (312) 321-4719.

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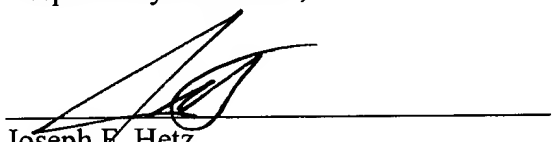
Respectfully submitted,



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